WHAT CLAIMED IS:

1. An integrated circuit system having a plurality of macros, said integrated circuit comprising:

an external voltage supply input configured for supplying an external voltage to the integrated circuit; and

a plurality of internal voltage supply generators, each of the plurality of internal voltage supply generators being connected to a respective macro of the plurality of macros and configured for receiving the external voltage via the external voltage supply input for generating an internal voltage supply for operating its respective macro, wherein each of the plurality of internal voltage supply generators includes circuitry for generating the internal voltage supply and circuitry for disconnecting at least a portion of its respective macro.

2. The integrated circuit system as in claim 1, wherein each of the plurality of internal voltage supply generators regulate the internal voltage supply generated there from.

3. The integrated circuit system as in claim 1, wherein the external voltage is greater than the internal voltage supply.

4. The integrated circuit system as in claim 1, further comprising a scan-chain formed by a chain of scannable register latches storing fuse information and a switch enable/disable signal.

5. The integrated circuit system as in claim 1, wherein each of the plurality of internal voltage supply generators comprise a reference voltage generator for generating and providing a reference voltage for driving at least one voltage generator.

6. The integrated circuit system as in claim 6, wherein the reference voltage generator and the at least one voltage generator provide voltage to a substrate bias level voltage generator, a negative word line level voltage generator, and a boosted wordline high level voltage generator.

7. The integrated circuit system as in claim 1, wherein the circuitry for generating the internal voltage supply comprises:

a reference supply unit for generating at least one of a voltage level and current level;

a voltage limiter coupled to the reference supply unit for controlling a voltage output level outputted from the voltage limiter;

an oscillator coupled to the voltage limiter for receiving the voltage output level and generating an oscillating voltage level; and

a charge pump for receiving the oscillating voltage level for generating the internal voltage supply.

8. The integrated circuit system as in claim 7, wherein a feedback voltage is provided from the charge pump to the voltage limiter.

9. The integrated circuit system as in claim 7, wherein the external voltage drives the reference supply unit, the voltage limiter, the oscillator, and the charge pump.

10. The integrated circuit system as in claim 7, wherein the circuitry for generating the internal voltage supply further comprises an enable register coupled to the voltage limiter, the oscillator and the charge pump, wherein the enable register is configured for storing one of an enable and disable signal and for enabling or disabling at least the voltage limiter, the oscillator and the charge pump according to the stored signal.

11. The integrated circuit system as in claim 10, wherein the enable register stores one of the enable and disable signal during a power-on period.

12. An integrated circuit system having a plurality of macros, said integrated circuit comprising:

means for receiving an external voltage;

means coupled to the means for receiving the external voltage for generating an internal voltage supply for operating at least one of a plurality of internal voltage supply generators coupled to a respective macro of the plurality of macros; and

means for controlling the means coupled to the means for receiving the external voltage according to an enable/disable signal to selectively connect and disconnect at least a portion of the respective macro of the plurality of macros.

13. The integrated circuit system as in claim 12, further comprising a scan-chain formed by a chain of scannable register latches storing fuse information and the enable/disable signal.

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14. The integrated circuit system as in claim 12, wherein the means coupled to the means for receiving the external voltage comprise a reference voltage generator for generating and providing a reference voltage for driving at least one voltage generator.

15. The integrated circuit system as in claim 14, wherein the reference voltage generator and the at least one voltage generator provide voltage to the at least one of the plurality of internal voltage supply generators.

16. The integrated circuit system as in claim 12, wherein the at least one of the plurality of internal voltage supply generators is selected from the group consisting of a substrate bias level voltage generator, a negative word line level voltage generator, and a boosted wordline high level voltage generator.

17. The integrated circuit as in claim 12, wherein the means coupled to the means for receiving the external voltage comprises:

a reference supply unit for generating at least one of a voltage level and current level;

a voltage limiter coupled to the reference supply unit for controlling a voltage output level outputted from the voltage limiter;

an oscillator coupled to the voltage limiter for receiving the voltage output level and generating an oscillating voltage level; and

a charge pump for receiving the oscillating voltage level for generating the internal voltage supply.

18. The integrated circuit system as in claim 17, wherein a feedback voltage is provided from the charge pump to the voltage limiter.

19. The integrated circuit system as in claim 17, wherein the external voltage drives the reference supply unit, the voltage limiter, the oscillator, and the charge pump.

20. The integrated circuit system as in claim 17, wherein the means for controlling the means coupled to the means for receiving the external voltage according to the enable/disable signal comprises at least one enable register coupled to the voltage limiter, the oscillator and the charge pump, wherein the at least one enable register is configured for storing the enable/disable signal and for enabling or disabling at least the voltage limiter, the oscillator and the charge pump according to the stored enable/disable signal.

21. The integrated circuit system as in claim 12, wherein at least one enable register stores the enable/disable signal during a power-on period.

22. The integrated circuit system as in claim 20, further comprising means for performing a built-in self test for testing the DC voltage generator system.